Copy 1

	L #	Hits	Search Text	DBs
1	L1	13	(result meaning) near10 decod$3 near10 (instruction command) near20 (depend$3 based alter$3 modif$6 chang$3) near10 mode near10 (flag bit register)	USPAT; US-PGPUB
2	L3	24	decod$3 near10 (instruction command) near20 (depend$3 based alter$3 modif$6 chang$3) near10 mode near10 (flag bit register)	EPO; JPO; DERWENT; IBM_TDB
3	L2	91	decod$3 near10 (instruction command) near20 (depend$3 based alter$3 modif$6 chang$3) near10 mode near10 (flag bit register)	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
1	JP 20010 35158 A	☐	METHOD AND SYSTEM FOR ACCESSING MEMORY	
2	JP 10171 441 A	☐	CHARACTER DISPLAY CONTROL CIRCUIT	
3	JP 08234 979 A	☐	PROCESSOR HAVING BRANCH INSTRUCTION EXECUTING FUNCTION AND BRANCH INSTRUCTION CONTROL METHOD	
4	JP 04254 985 A	☐	DRAM CONTROLLER	
5	JP 04102 982 A	☐	MICROCOMPUTER	
6	JP 01283 647 A	☐	DUPLICATED ERROR GENERATING DEVICE FOR MICROPROCESSOR	
7	JP 01037 627 A	☐	REGISTER UPDATING MECHANISM	
8	JP 60096 030 A	☐	DECODING SYSTEM	
9	JP 59003 642 A	☐	CONTROL REGISTER PROCESSING SYSTEM	
10	JP 57059 205 A	☐	NUMERIC CONTROLLER	
11	JP 56074 749 A	☐	MICROPROGRAM CONTROLLING DEVICE	
12	DE 19932 465 C1	☐	Arrangement for programming functional devices equipped with digital decoders changes decoder to programming mode using drive voltage on track with digital controller in reset state	
13	EP 10507 98 A1	☐	Decoding instructions	
14	DE 19932 465 C	☐	Arrangement for programming functional devices equipped with digital decoders changes decoder to programming mode using drive voltage on track with digital controller in reset state	
15	EP 10507 98 A	☐	Decode unit for decoding instructions in a processor that can support three instruction modes has detector that temporarily allows first length instructions to be decoded without changing instruction mode held in register	
16	US 60121 38 A	☐	Dynamically variable length CPU pipeline for executing multiple instruction sets	
17	JP 11154 393 A	☐	Non-volatile semiconductor memory e.g. electrically erasable programmable read only memory EEPROM, used for recording of multimedia information - has controller which makes predetermined number as designated page unit when predetermined command for designating program unit is included based on decoding result of command decoder	
18	US 58023 60 A	☐	Integrated circuit with digital processor for dynamic selection of instruction execution intervals - has decode stage coupled to execute stage with mode input for selecting number of clock cycles taken to execute flag-modifying instruction	
19	US 51230 96 A	☐	Data processor with addressing mode decoding function - modifies entry address of microinstruction when addressing mode of operand detected to enable entry address	
20	JP 02011 076 A	☐	Sound decoder for MUSE television receiver - operates muting circuit when state change of mode command bit in control code is detected NoAbstract Dwg 0/2	

	Document ID	U	Title	Current OR
21	DE 3500741 A	☐	Integrated circuit for floppy disc drive control - has registers to handle control and data transfers between disc drive and computer operating with status interlock stage	
22	SU 1065852 A	☐	Multi-computer network computer interfacing unit - has memory data input coupled through high-way with coupling amplifier data outputs to group lines	
23	WO 8303017 A	☐	Computer with static cache - automatically maps memory contents into machine registers during program execution	
24	EP 40703 A	☐	Enhancement of 370 type data processor - reduces overhead incurred by multiple users by permitting program in one address space to obtain access to data in another address space	

	Document ID	U	Title	Current OR
1	US 20030021163 A1	☐	Semiconductor memory device and information device	365/189.12
2	US 20010007541 A1	☐	Semiconductor memory device	365/233
3	US 20010005132 A1	☐	Semiconductor device testing method and system and recording medium	324/158.1
4	US 6617842 B2	☐	Semiconductor device testing method and system employing trace data	324/158.1
5	US 6549475 B2	☐	Semiconductor memory device and information device	365/189.12
6	US 6504789 B2	☐	Semiconductor memory device	365/233
7	US 6425047 B1	☐	Process containing address decoders suited to improvements in clock speed	711/101
8	US 5761490 A	☐	Changing the meaning of a pre-decode bit in a cache memory depending on branch prediction mode	712/239
9	US 5506970 A	☐	Bus arbitrator circuit	710/113
10	US 5412784 A	☐	Apparatus for parallelizing serial instruction sequences and creating entry points into parallelized instruction sequences at places other than beginning of particular parallelized instruction sequence	712/245
11	US 5408658 A	☐	Self-scheduling parallel computer system and method	712/216
12	US 5347639 A	☐	Self-parallelizing computer system and method	712/203
13	US 4414622 A	☐	Addressing system for a computer, including a mode register	711/215

	Document ID	U	Title	Current OR
1	US 20040019756 A1	☐	Memory device supporting a dynamically configurable core organization	711/170
2	US 20030223293 A1	☒	Synchronous type semiconductor memory device	365/200
3	US 20030164510 A1	☒	Redundancy architecture for repairing semiconductor memories	257/200
4	US 20030135779 A1	☒	Microprocessor	713/600
5	US 20030126529 A1	☒	Wafer burn-in test mode circuit	714/720
6	US 20030101333 A1	☒	Data processor	712/226
7	US 20030085731 A1	☒	Semiconductor device having test mode entry circuit	326/16
8	US 20030081491 A1	☒	SEMICONDUCTOR MEMORY DEVICE WITH REDUCED POWER CONSUMPTION	365/233
9	US 20030075789 A1	☒	Semiconductor storage device having memory chips in a stacked structure	257/678
10	US 20030061536 A1	☒	Power controlling method for semiconductor storage device and semiconductor storage device employing same	714/14
11	US 20030021163 A1	☐	Semiconductor memory device and information device	365/189.12
12	US 20030014457 A1	☒	Method and apparatus for vector processing	708/520
13	US 20020171075 A1	☒	Register setting method and semiconductor device	257/10
14	US 20020145929 A1	☒	Control circuit and semiconductor memory device	365/222
15	US 20010023424 A1	☒	Exponent unit of data processing system	708/277
16	US 20010007541 A1	☐	Semiconductor memory device	365/233
17	US 20010005132 A1	☐	Semiconductor device testing method and system and recording medium	324/158.1

	Document ID	U	Title	Current OR
18	US 6678818 B1	☒	Decoding next instruction of different length without length mode indicator change upon length change instruction detection	712/210
19	US 6675290 B1	☒	Processor for improving instruction utilization using multiple parallel processors and computer system equipped with the processor	712/229
20	US 6651196 B1	☒	Semiconductor device having test mode entry circuit	714/724
21	US 6631463 B1	☒	Method and apparatus for patching problematic instructions in a microprocessor using software interrupts	712/227
22	US 6617842 B2	☐	Semiconductor device testing method and system employing trace data	324/158.1
23	US 6577550 B2	☒	Control circuit and semiconductor memory device	365/222
24	US 6574727 B1	☒	Method and apparatus for instruction sampling for performance monitoring and debug	712/227
25	US 6566760 B1	☒	Semiconductor storage device having memory chips in a stacked structure	257/777
26	US 6552955 B1	☒	Semiconductor memory device with reduced power consumption	365/233
27	US 6549991 B1	☒	Pipelined SDRAM memory controller to optimize bus utilization	711/158
28	US 6549475 B2	☐	Semiconductor memory device and information device	365/189.12
29	US 6539502 B1	☒	Method and apparatus for identifying instructions for performance monitoring in a microprocessor	714/47
30	US 6504789 B2	☐	Semiconductor memory device	365/233
31	US 6492992 B2	☒	Graphic pattern processing apparatus	345/568
32	US 6487629 B1	☒	Semiconductor memory for operation in a plurality of operational modes	711/104
33	US 6463518 B1	☒	Generation of memory addresses for accessing a memory utilizing scheme registers	711/220
34	US 6453278 B1	☒	Flexible implementation of a system management mode (SMM) in a processor	703/27
35	US 6426560 B1	☒	Semiconductor device and memory module	257/777
36	US 6425047 B1	☐	Process containing address decoders suited to improvements in clock speed	711/101
37	US 6414530 B2	☒	Semiconductor integrated circuit device, semiconductor memory system and clock synchronous circuit	327/269
38	US 6381720 B1	☒	Test circuit and method for system logic	714/727
39	US 6381690 B1	☒	Semiconductor memory device in which use of cache can be selected	365/230.03
40	US 6336178 B1	☒	RISC86 instruction set	712/23

	Document ID	U	Title	Current OR
41	US 6292848 B1	☒	Computing system adapter card for supporting legacy and plug and play configurations	710/8
42	US 6208563 B1	☒	Semiconductor memory device which continuously performs read/write operations with short access time	365/189.05
43	US 6141742 A	☒	Method for reducing number of bits used in storage of instruction address pointer values	711/220
44	US 6093213 A	☒	Flexible implementation of a system management mode (SMM) in a processor	703/27
45	US 6085314 A	☒	Central processing unit including APX and DSP cores and including selectable APX and DSP execution modes	712/213
46	US 6081886 A	☒	Holding mechanism for changing operation modes in a pipelined computer	712/229
47	US 6032247 A	☒	Central processing unit including APX and DSP cores which receives and processes APX and DSP instructions	712/35
48	US 6014714 A	☒	Adapter card system including for supporting multiple configurations using mapping bit	710/8
49	US 5991531 A	☒	Scalable width vector processor architecture for efficient emulation	703/26
50	US 5973988 A	☒	Semiconductor memory device having circuit for monitoring set value of mode register	365/230.08
51	US 5926642 A	☒	RISC86 instruction set	712/1
52	US 5925123 A	☒	Processor for executing instruction sets received from a network or from a local memory	712/212
53	US 5920713 A	☒	Instruction decoder including two-way emulation code branching	712/236
54	US 5909567 A	☒	Apparatus and method for native mode processing in a RISC-based CISC processor	712/208
55	US 5893927 A	☒	Memory device having programmable device width, method of programming, and method of setting device width for memory device	711/171
56	US 5854913 A	☒	Microprocessor with an architecture mode control capable of supporting extensions of two distinct instruction-set architectures	712/210
57	US 5852428 A	☒	Display driving device	345/100
58	US 5819056 A	☒	Instruction buffer organization method and system	712/204
59	US 5809273 A	☒	Instruction predecode and multiple instruction decode	712/210
60	US 5802360 A	☒	Digital microprocessor device having dnamically selectable instruction execution intervals	712/229
61	US 5794063 A	☒	Instruction decoder including emulation using indirect specifiers	712/23
62	US 5793775 A	☒	Low voltage test mode operation enable scheme with hardware safeguard	714/724
63	US 5781750 A	☒	Dual-instruction-set architecture CPU with hidden software emulation mode	712/209

	Document ID	U	Title	Current OR
64	US 5761490 A	☐	Changing the meaning of a pre-decode bit in a cache memory depending on branch prediction mode	712/239
65	US 5703616 A	☒	Display driving device	345/98
66	US 5663745 A	☒	Display driving device	345/98
67	US 5636173 A	☒	Auto-precharge during bank selection	365/230.03
68	US 5630161 A	☒	Serial-parallel digital signal processor	712/36
69	US 5560036 A	☒	Data processing having incircuit emulation function	712/227
70	US 5530804 A	☒	Superscalar processor with plural pipelined execution units each unit selectively having both normal and debug modes	714/30
71	US 5506970 A	☐	Bus arbitrator circuit	710/113
72	US 5412784 A	☐	Apparatus for parallelizing serial instruction sequences and creating entry points into parallelized instruction sequences at places other than beginning of particular parallelized instruction sequence	712/245
73	US 5408658 A	☐	Self-scheduling parallel computer system and method	712/216
74	US 5396498 A	☒	Integrated circuit with peripheral test controller	714/703
75	US 5347639 A	☐	Self-parallelizing computer system and method	712/203
76	US 5280593 A	☒	Computer system permitting switching between architected and interpretation instructions in a pipeline by enabling pipeline drain	712/208
77	US 5226164 A	☒	Millicode register management and pipeline reset	712/209
78	US 5167026 A	☒	Simultaneously or sequentially decoding multiple specifiers of a variable length pipeline instruction based on detection of modified value of specifier registers	712/210
79	US 5148528 A	☒	Method and apparatus for simultaneously decoding three operands in a variable length instruction when one of the operands is also of variable length	712/210
80	US 5142633 A	☒	Preprocessing implied specifiers in a pipelined processor	712/225
81	US 5129079 A	☒	Computer system having subinstruction surveillance capability	712/211
82	US 5123096 A	☒	Data processor with addressing mode decoding function	712/212
83	US 5031096 A	☒	Method and apparatus for compressing the execution time of an instruction stream executing in a pipelined processor	711/169
84	US 4561443 A	☒	Coherent inductive communications link for biomedical applications	607/31
85	US 4414622 A	☐	Addressing system for a computer, including a mode register	711/215

	Document ID	U	Title	Current OR
86	US 4344129 A	☒	Data processor system capable of providing both a computer mode and a sequencer mode of operation	712/229
87	US 4199810 A	☒	Radiation hardened register file	714/15
88	US 4107781 A	☒	Electronic calculator or microprocessor with indirect addressing	708/100
89	US 4084235 A	☒	Emulation apparatus	703/26
90	US 3818460 A	☒	EXTENDED MAIN MEMORY ADDRESSING APPARATUS	711/2
91	US 3577190 A	☐	APPARATUS IN A DIGITAL COMPUTER FOR ALLOWING THE SKIPPING OF PREDETERMINED INSTRUCTIONS IN A SEQUENCE OF INSTRUCTIONS, IN RESPONSE TO THE OCCURRENCE OF CERTAIN CONDITIONS	712/226